Amendments to the Specification:

Please replace paragraph [0005] with the following amended paragraph:

[0005] A first aspect of the present invention is an electronic device comprising: a semiconductor device comprising: a pass gate transistor including a first fin body and a first gate, the first fin body having opposing sidewalls, each sidewall aligned in a first direction having a first majority carrier mobility, the first gate adjacent to both sidewalls of the first fin body; a pull down latch transistor including a second fin body and a second gate, the second fin body having opposing sidewalls, each sidewall aligned in a second direction having a second majority carrier mobility, the second gate adjacent to both sidewalls of the second fin body; a pull up latch transistor including a third fin body and a third gate, the third fin body having opposing sidewalls, each sidewall aligned in a third direction having a [[first]] <u>third</u> majority carrier mobility, the third gate adjacent to both sidewalls of the third fin body; wherein all of the first, second and third directions are not the same direction; and one or more CMOS chevron logic circuits, crystal planes of bodies of transistors of the CMOS chevron logic circuits and crystal planes of the first, second and third fin bodies co-aligned.

Please replace paragraph [0006] with the following amended paragraph:

[0006] A second aspect of the present invention is a method of fabricating a semiconductor device comprising: forming a first fin body of a pass gate transistor from a crystal layer, the first fin body having opposing sidewalls, each sidewall aligned in a first direction having a first majority carrier mobility; forming a second fin body of a ~~pass gate~~ <u>pull down latch</u> transistor from the crystal layer, the second fin body having opposing sidewalls, each sidewall aligned in a second direction having a second majority carrier mobility; forming a third fin body of a ~~pass gate~~ <u>pull up latch</u> transistor from the crystal layer the third fin body having opposing

sidewalls, each sidewall aligned in a first direction having a third majority carrier mobility; and forming a first gate adjacent to both sidewalls of the first fin body, a second gate adjacent to both sidewalls of the second fin body and a third gate adjacent to both sidewalls of the third fin body wherein all of the first, second and third directions are not the same direction; and forming bodies of CMOS devices of one or more CMOS chevron logic circuits from the crystal layer.

Please replace paragraph [0006] with the following amended paragraph:

[0006] A third aspect of the present invention is an electronic device comprising: an SRAM cell comprising: first and second pass gate transistors, each pass gate transistor including a fin body and a gate, the first fin bodies each having opposing sidewalls and each sidewall aligned in a first direction having a first majority carrier mobility, the gate adjacent to both sidewalls; first and second pull down latch transistors, each pull down transistor including a fin body and a gate, each fin body having opposing sidewalls and each sidewall aligned in a second direction having a second majority carrier mobility, the gate adjacent to both sidewalls; first and second pull up latch transistors, each latch transistor including a fin body and a gate, each fin body having opposing sidewalls and each sidewall aligned in a third direction having a third majority carrier mobility, the gate adjacent to both sidewalls, the third direction aligned between a {100} crystal plane and a {110} crystal plane of the fin bodies of the first and second pull up latch transistors; and wherein all of the first, second and third directions are not the same direction; and one or more CMOS chevron logic circuits, crystal planes of bodies of transistors of the CMOS chevron logic circuits ~~and crystal planes of the first, second and third fin bodies~~ co-aligned with crystal planes of the fin bodies of the pass gate transistors, the pull down latch transistors and the pull up latch transistors.

Please replace paragraph [0039] with the following amended paragraph:

[0039] The major axes 285 of each fin 255 are orientated at an angle of 22.5° from a reference line 290, which bisects a notch 295. Major axes 285 are aligned along a {100} crystal plane. Thus, channel regions 300 (defined by the overlap of gate 260 with fins 255) of NFETs 250 are orientated along a ~~{110}~~ {100} crystal plane and NFETs 250 have a high majority carrier mobility and high drive.

Please replace paragraph [0045] with the following amended paragraph:

[0045] FIG. 8 is a diagram illustrating the relationship between four adjacent SRAM cells according to the present invention. SRAM cells are usually designed mirrored in two directions in order to increase density. In FIG. 8, a repeating SRAM pattern 315 includes SRAM cells 320A, 320B, 320C and 320D. SRAM cell 320A has corners A, B, C and D. SRAM cell 320B is a mirror image of SRAM cell 320A mirrored along a horizontal axis 325. SRAM cell [[320B]] 320D is a mirror image of SRAM cell 320C mirrored along horizontal axis 325. SRAM cell 320C is a mirror image of SRAM cell 320A mirrored along a vertical axis 330. SRAM cell 320D is a mirror image of SRAM cell 320B mirrored along vertical axis 330. A complete SRAM array includes a multiplicity of SRAM patterns 315 tiled in the vertical and/or horizontal direction. Thus, a description of the layout of SRAM cell 320A suffices to describe the layouts of SRAM cells 320B, 320C and 320D.

Please replace paragraph [0047] with the following amended paragraph:

[0047] FIG. 9 is diagram illustrating the layout of an SRAM cell 320A1 according to a first embodiment of the present invention. In FIG. 9 a vertical axis 330A is parallel to vertical axis 330 that passes through notch 335. Vertical axis 330A is orientated 22.5° clockwise from the {100} crystal plane and 22.5° counterclockwise from the {110} crystal ~~planes~~ plane. In FIG. 9, SRAM cell 320A1 includes a first pass gate NFET N3 comprising a fin 340A and a gate 345, a second pass gate NFET N4 comprising a fin 350A and a gate 355, a first pull up ~~NFET~~ PFET

P1 comprising a fin 360 and a common gate 365, a first pull down NFET N1 comprising a fin 340B and common gate 365, a second pull up PFET P2 comprising a fin 370 and a common gate 375, and a second pull down NFET N2 comprising a fin 350B and common gate 375. Fins 340A and 340B are coextensive and fins 350A and 350B are coextensive.

Please replace paragraph [0050] with the following amended paragraph:

[0050] FIG. 10 is diagram illustrating the layout of an SRAM cell 320A2 according to a second embodiment of the present invention. In FIG. 10 a vertical axis 330A is parallel to vertical axis 330 that passes through notch 335. Vertical axis 330A is orientated 22.5° clockwise from the {100} crystal plane and 22.5° counterclockwise from the {110} crystal ~~planes~~ plane. In FIG. 10, SRAM cell 320A2 includes a first pass gate NFET N3 comprising a fin 440A and a gate 445, a second pass gate NFET N4 comprising a fin 450A and a gate 455, a first pull up ~~NFET~~ PFET P1 comprising a fin 460 and a common gate 465, a first pull down NFET N1 comprising a fin 440B and common gate 465, a second pull up PFET P2 comprising a fin 470 and a common gate 475, and a second pull down NFET N2 comprising a fin 450B and common gate 475. Fins 440A and 440B are coextensive and fins 450A and 450B are coextensive.

Please replace paragraph [0051] with the following amended paragraph:

[0051] Fins 440A, 450A, 460 and 470 are orientated 90° from vertical axis 330A which is 22.5 degrees from the {100} or {110} crystal planes, thus providing medium majority carrier mobility (as defined *supra*) for pass gate NFETs N3 and N4 [[,]] and pull up PFETS P1 and P2. Fins 440B and 450B are orientated 67.5° from vertical axis 330A, which is on the {100} crystal plane, thus providing high majority carrier mobility (as defined *supra*) for pull down NFETs N1 and N2. The layout of SRAM 320A2 allows a medium performance SRAM (since majority carrier mobility in pull down NFETs [[N3]] N1 and [[N4]] N2 is high but majority carrier mobility in pass gates NFETs N3 and N4 is medium) having a relatively medium density (since

length L3 is driven by groundrules and the extra space required to lay out fins 440B and 450B along a diagonal) as compared to the first and second embodiments of the present invention. SRAM cell 320A3 may be used with standard CMOS logic technology or may be easily integrated with chevron CMOS logic technology as defined *supra*.

Please replace paragraph [0053] with the following amended paragraph:

[0053] FIG. 11 is a diagram illustrating the layout of an SRAM cell 320A3 according to a first alternative of a third embodiment of the present invention. In FIG. 11 a vertical axis 330A is parallel to vertical axis 330 that passes through notch 335. Vertical axis 330A is orientated 22.5° clockwise from the {100} crystal plane and 22.5° counterclockwise from the {110} crystal ~~planes~~ plane. In FIG. 11, SRAM cell 320A3 includes a first pass gate NFET N3 comprising a fin 540A and a gate 545, a second pass gate NFET N4 comprising a fin 550A and a gate 555, a first pull up ~~NFET~~ PFET P1 comprising a fin 560 and a common gate 565, a first pull down NFET N1 comprising a fin 540B and common gate 565, a second pull up PFET P2 comprising a fin 570 and a common gate 575, and a second pull down NFET N2 comprising a fin 550B and common gate 575. Fins 540A and 540B are coextensive and fins 550A and 550B are coextensive.

Please replace the abstract] with the following amended abstract:

[[A]] An electronic device, and SRAM and a method of forming the electronic device and SRAM. (Original) The semiconductor device including: a pass gate transistor having a fin body having opposing sidewalls aligned in a first direction and having a first majority carrier mobility and a gate adjacent to both sidewalls of the fin body; a pull down latch transistor having a fin body having opposing sidewalls aligned in a ~~first~~ second direction and having a ~~first~~ second majority carrier mobility and a gate adjacent to both sidewalls of the fin body; a pull up latch transistor having a fin body having opposing sidewalls aligned in a ~~first~~ third direction and

having a ~~first~~ third majority carrier mobility and a gate adjacent to both sidewalls of the fin body; and CMOS chevron logic circuits, wherein crystal planes of each fin body and of CMOS transistor of the chevron logic are co-aligned.